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10/673,434

09/30/2003

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EXAMINER

PHAN, THIEM D

ART UNIT

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3729

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/673,434	<b>Applicant(s)</b> YOKOYAMA ET AL.	
	<b>Examiner</b> THIEM PHAN	<b>Art Unit</b> 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 4,7,9 and 10 is/are pending in the application.
- 4a) Of the above claim(s) 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 4,7,9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. The Amendment filed on 4/11/08 has been fully considered and made of record.
2. Applicants' Amendment (filed 4/11/08) has added new embodiment, which then necessitates new grounds of Restriction presented in this Office action.

Restriction to one of the following inventions is required under 35 U. S. C. 121:

- I. Claims 4, 7 and 9, drawn to a method of manufacturing a battery pack, classified in class 29, subclass 825;
  - II. Claim 10, drawn to another method of manufacturing a battery pack, classified in class 29, subclass 842.
3. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the method of manufacturing a battery pack as recited in Group I does not require a second area thereof, as required by Group II. The subcombination, Invention II, has separate utility such as forming an insulating in a first area.

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4. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicants are advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicants traverse on the ground that the inventions are not patentably distinct, applicants should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

5. Since applicants have received an action on the merits for the originally presented or claimed invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 10 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants are required to cancel these nonelected claim (10) or take other appropriate action.

An Office Action on the merits of Claims 4, 7 and 9 now follows.

### ***Claim Objections***

6. There is an improper claims cancellation in page 3: "Claims 8-10 (Cancelled)". Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being anticipated by Shoji et al (US 5,982,629).

**Regarding claim 4**, Shoji et al teach a method of fabricating a circuit board (Col. 3, lines 29+; col. 6, lines 36-40 where the item 1 of Fig. 1 to 6 can be interpreted as of a printed circuit board or component chip), comprising the steps of:

- a step of forming a terminal portion (Fig. 1, 2) in manufacturing a square-shaped circuit board (Fig. 1, 1; col. 7, line 40), said step of forming a terminal portion being to stack a base layer of copper or Cu (Fig. 1, 2; col. 4, lines 45-48) and a plated layer of gold or Au (Fig. 1, 3; col. 2, lines 45 & 46) successively to form the terminal portion; except for having the circuit board made of glass epoxy resin; and
- a step of forming an insulating layer (Fig. 9, 5) after said step of forming a terminal portion in manufacturing said circuit board, said step of forming an insulating layer being to form an insulating layer in the other area than the area where said terminal portion (Fig. 9, 2) is formed,
- wherein said insulating layer is formed so as to cover a peripheral edge of said plated layer (Fig. 9, 3; col. 5, lines 28-30) so that the surface of said circuit board and at least

one of the surface of the base layer (Fig. 9, 2) are not exposed externally, and the insulating layer (Fig. 9, 5; col. 11, lines 38 & 39) is made of epoxy resin or the like; and

- a step of mounting an electronic component (Fig. 7, item 11 is construed as component due to similar process forming bump on component or wiring board; col. 6, lines 36-49) after the step of forming the insulating layer, the step of mounting the electronic component including mounting the electronic component on given position of the circuit board by a solder reflow process (Fig. 7, 8 & 13; col. 9, lines 50 & 51).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have the circuit board made of glass epoxy resin because applicants have not disclose that having the circuit board made of glass epoxy resin provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with a silicon substrate material (Abstract) because it insulates and supports the conductive regions (Fig. 1, 2 & 3) as well.

Therefore, it would have been an obvious matter of design choice to modify Shoji et al to obtain the invention as specified in Claim 4.

**Regarding claim 7**, Shoji et al teach the further steps of:

- forming a base layer of a copper pattern (Fig. 1, 2) on a surface of an insulating board (Fig. 1, 1);
- forming a plated layer (Fig. 1, 3) so as to cover the entire base layer (Fig. 1, 2) by selective plating (Col. 5, line 5); and

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- forming an insulating layer (Fig. 9, 5) on said plated layer (Fig. 9, 3) and patterning said insulating layer so that only a portion of said plated layer is exposed externally.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being anticipated by Shoji et al in view of Mita et al (US 6,297,142).

Shoji et al teach a method of fabricating a circuit board, which reads on applicants'

claimed invention; except for stamping out a rigid-type integral along each area, on which the circuit board is to be formed, with a mold.

Mita et al teach a method of forming semiconductor chip (Figs. 10A-11D; 1) by stamping out a rigid-type integral along each area of the TAB (Fig. 11A, 6) on which the circuit board is to be formed, with a mold (Fig. 11D, S805; col. 6, lines 43-45), in order to mass produce the chip components.

It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Shoji et al by applying the stamping process, as taught by Mita et al, in order to mass produce the chip components.

### ***Response to Arguments***

10. Applicants' arguments filed on 4/11/08 have been fully considered but they are not persuasive.

Applicants' assertions of the reason for using the circuit board as glass epoxy resin and the insulation layer as epoxy resin in order to avoid any peeling off (Remarks, page 6, 2<sup>nd</sup>



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paragraph – page 7) are traversed because these reasons are nowhere to be found in the original specification or drawings and the rejection by design choice of these compositions is provided because applicants have not disclosed that having the circuit board made of glass epoxy resin provides an advantage, is used for a particular purpose, or solves a stated problem. Therefore, the circuit board made of silicon substrate (Fig. 3, 1; Abstract) and the insulation layer made of polyimide resin (Fig. 3, 5; col. 11, line 39), as taught by Shoji et al, can very well insulate and support the conductive region (Fig. 3, 2 & 3) without any peeling off.

Applicants further assert that the materials taught by the prior art Shoji et al would peel off (Remarks, page 6, 1<sup>st</sup> paragraph). In responses to these remarks, Shoji et al teach the circuit board as of silicon substrate (Fig. 3, 1; Abstract) with the insulation layer as polyimide resin (Fig. 3, 5; col. 11, line 39) and these two materials would adhere to each other without being peeled off.

Moreover, the claimed limitation "... glass epoxy resin ..." (Claim 4, line 8), "... epoxy resin;" (Claim 4, line 15) is considered to be of Composition Claim while the current, claimed invention is about the Method Claims where the process of manufacturing a circuit board of battery pack operates and does not depend on the composition limitation for completeness but, instead, the process steps or limitations are able to stand alone so this manner of operation does not distinguish over the process of Shoji et al, and Shoji et al at a minimum suggest the claimed method invention.

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Applicants' amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phan Thiem/

Tim Phan  
Examiner  
Art Unit 3729

July 9, 2008